

## **A 0.45um-pitch Photodiode Based 1-layer Dual Pixel for CMOS Image Sensor with High Full-Well Capacity and Low Noise**

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### **Abstract**

In this paper, we developed the 0.9um (0.45um×0.9um×2) dual pixel-based tetra CMOS image sensor (CIS) with full-depth deep trench isolation (FDTI). In spite of the reduced pixel area, characteristics are similar to the 1.0um based FDTI dual pixel by incorporating the novel isolation structure. We implemented asymmetric deep trench isolation (DTI) which led to the simultaneous improvement of high full well capacity (FWC) over 16,000e- and in-pixel overflow path with preserving signal linearity. In addition, the inevitable coupling problem between adjacent pixels according to the pixel shrink is completely restrained by the contact wall isolation structure.

### **Introduction**

High resolution and auto-focus (AF) density has been required in recent smartphone camera models [1]. Although these features can be simultaneously achieved with small pitch based dual pixel, the shrinkage of pixel induce inevitable performance degradation, thereby requiring the structure alteration for image quality [2, 3].

If the existing structure is maintained, the shrinkage of photodiode (PD) under sub-micron in 1-layer dual pixel can induce the following problems: limitation of high FWC due to the narrowed n-type photodiode and the diffused p-type plasma-assisted doping as shown in Fig.1, coupling noise due to the reduced distance between adjacent pixels, and vulnerable to leakage noise due to the decreased distance between floating diffusion node and transfer gate (TG).

In order to overcome narrow limitations, we developed asymmetric deep trench and contact wall isolation with dual vertical TG, and consequentially obtained 60% enhanced FWC and improved coupling noise despite the pixel shrinkage from 1.0um to 0.9um.

### **Asymmetric DTI for high FWC**

The dual pixel consisted of left PD and right PD to acquiring a PDAF signal, requires an inter-PD overflow (IPO) charge path to maintain signal linearity [4, 5]. As pixel shrinks, the reduced DTI width for higher FWC induces the insufficient IPO level by strengthening n-type doping around the internal DTI. Because IPO level of the dual pixel is determined by the p-type implantation on the DTI interface and the n-type photodiode, it is substantially formed at the center of internal DTI cut. If the internal DTI width is reduced, it is impossible to increase the IPO potential level unless the cut width is reduced because the n-dopant is relatively reinforced in the surrounding area. And this insufficient IPO level limits AF operation in a high illuminance environment, this should be formed at a low potential in the absence of linearity problem.

Fig. 2(a) shows the PD potential and IPO level of previous reported 1.0um dual pixel. Because the retention of DTI width limits FWC acquisition due to the reduced PD area, and the shrinkage of DTI induce the insufficient IPO level, we implemented the width of external DTI and internal DTI differently to secure a high FWC and an adequate IPO level. We performed technology computer aided design (TCAD) simulation according to the DTI structure, and confirmed the increased photodiode potential max (PDmax) and adequate IPO level by employing the proposed asymmetric DTI.

As a result, AF contrast is maintained even if relatively high signal is contained in left PD with proposed asymmetric DTI as shown in Fig. 2(b), and the linear FWC is remarkably increased to 16,000e- in comparison to the previous 1.0um dual pixel (Fig. 2(c)).

### **Contact wall isolation for low noise**

Secondly, as pixel shrinks, parasitic coupling effects can be inevitably occurred due to the decreased gap between adjacent neighboring FD nodes. In terms of metal routing with process limitation, the interval between neighboring FD nodes is not simply dropped as much as the shrinkage of pixel pitch. Fig. 3(a), (b) shows layout schemes of conventional FDTI dual pixel with pixel pitch and the proposed structure with contact wall is shown in Fig. 3(c). As the spacing becomes closer, due to the FD coupling effect, coupling noise is generated around bad pixels, causing defects cannot be corrected without CA wall.

Therefore, in order to minimize this coupling effect, we formed an additional contact between FD nodes, thereby hindering the coupling noise to under 0.12% as shown in Fig. 4(a, b). Coupling noise of adjacent left and right pixel increase depending on the signal of the seed pixel, but when using the suggested contact wall, it has improved more than the coupling noise of 1.0um dual pixel.

### **Conclusion**

We demonstrated a sub-micron dual pixel in 0.45um × 0.9um pitch with higher FWC and lower noise compared with previous 1.0um dual pixel by applying new isolation structure and transfer gate (Table. 1). In addition, AF contrast of 3.0 is achieved through the sufficiently formed deep photodiode and novel optical structure (Fig. 5). Furthermore, the contact wall structure presented in this paper effectively improve the coupling noise occurred at 0.45um pitch.

### **References**

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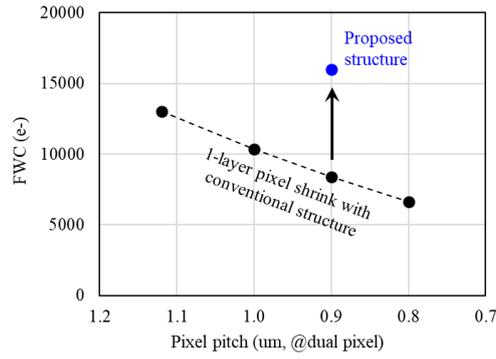


Figure 1. Full well capacity with pixel shrink under sub-micron dual pixel

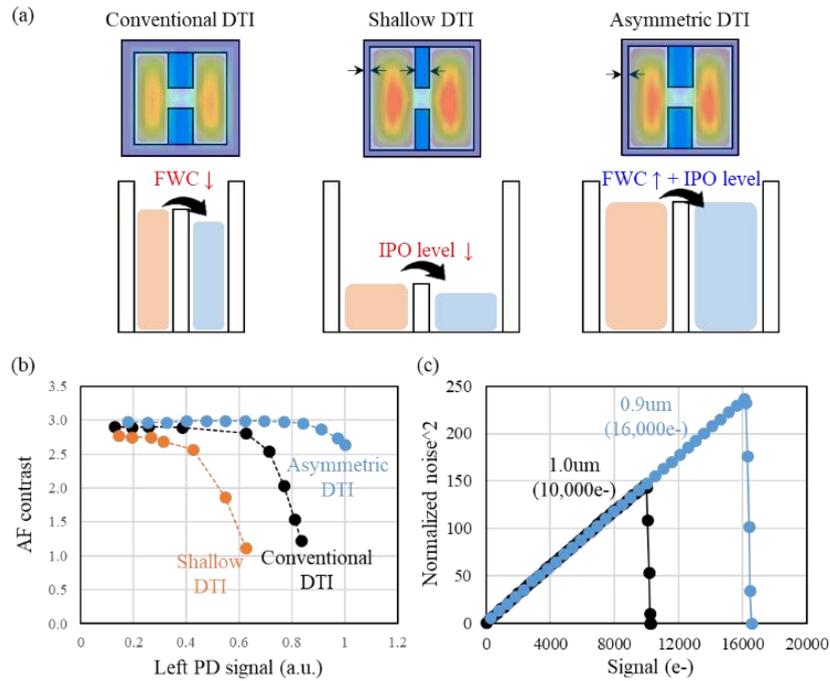


Figure 2. (a) IPO and FWC at small pixel with DTI concept, (b) AF contrast with photodiode signal, and (c) comparison of full well capacity

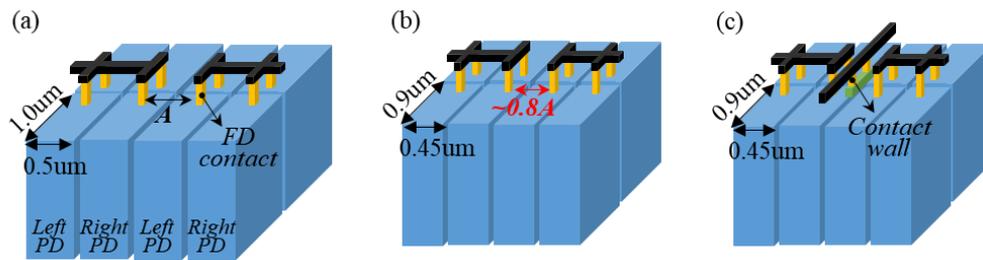


Figure 3. Layout scheme of conventional structure of (a) 1.0μm dual pixel, (b) 0.9μm, (c) proposed contact wall structure

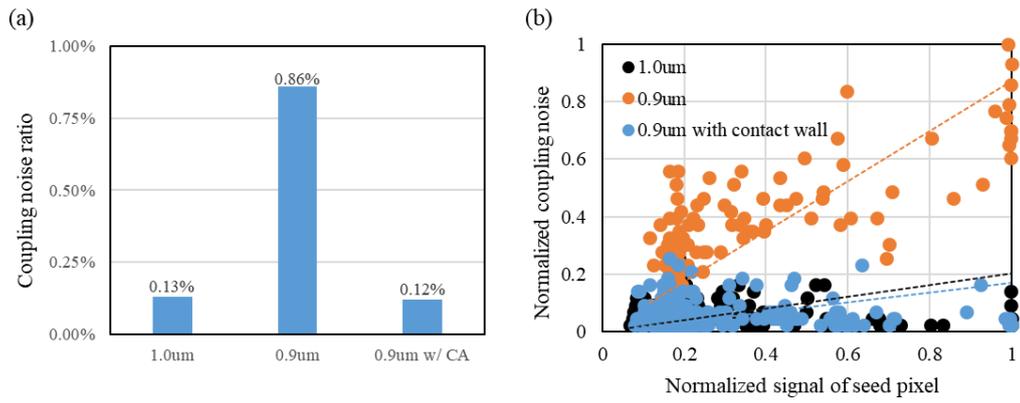


Figure 4. (a) Coupling noise ratio of 1.0um/0.9um/0.9um with contact wall and (b) relationship between the normalized signal of the seed pixel and the coupling noise

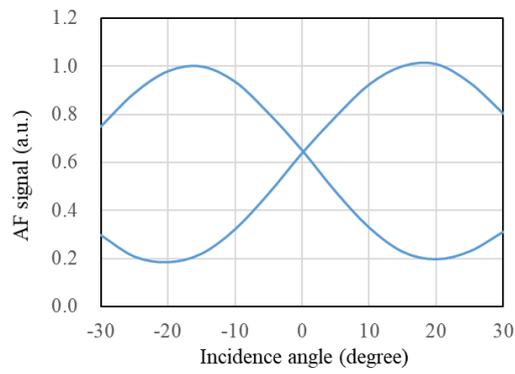


Figure 5. AF angular response of proposed 0.9um dual pixel

Table 1. Pixel performance summary of 0.9um dual pixel compared to previous 1.0um dual pixel

Items	Unit	1.0um FDTI dual Pixel	0.9um FDTI dual Pixel (This work)
Photodiode size	um	0.5 x 1.0	0.45 x 0.9
Full Well capacity	e-	10,000	16,000
FD coupling noise ratio	%	0.13	0.12
Random noise	A.U.	1	0.85
AF contrast	-	3.2	3.0